The listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (withdrawn) A method of forming a semiconductor structure comprising the steps of:
a) providing a semiconductor substrate;
b) providing a layer of SiGe over at least a region of the semiconductor substrate;
c) providing a mesa of over a portion of the SiGe layer;
d) depositing a polycrystalline silicon layer over the mesa and over lower adjacent regions of the SiGe layer;
e) planarizing the polycrystalline silicon layer to expose the mesa and,
f) etching the mesa to expose a region of SiGe below.

Claim 2 (withdrawn) A method as defined in claim 1, wherein the mesa is a SiO_xN_y material.

Claim 3 (withdrawn) A method as defined in claim 1, wherein step (e) is performed by polishing the polycrystalline silicon layer.

Claim 4 (withdrawn) A method as defined in claim 3, wherein the polishing is performed to expose a surface of the mesa.

Claim 5 (withdrawn) A method as defined in claim 1, wherein the step of etching etches away the mesa while substantially preserving the adjacent polysilicon SiGe layers.

Claim 6 (withdrawn) A method of forming a semiconductor structure comprising the steps of:
a) providing a substrate of a first semiconductor type;

b) providing a second layer of a second type of semiconductor material over at least a region of the first semiconductor substrate;
c) providing a mesa over a portion of the second layer, the mesa being a material that can bond to the second type of semiconductor and that can be etched by an etching source without etching the second type of semiconductor;
d) depositing a conductive layer over the mesa and over lower regions adjacent the mesa that will not be etched by the etching source;
e) planarizing the conductive layer; and,
f) etching the mesa to expose a region of the second layer below.

Claim 7 (withdrawn) A method as defined in claim 6, wherein the first semiconductor type is has a conductivity of a first type, and wherein the second layer of the second type of semiconductor material has a second conductivity type.

Claim 8 (withdrawn) A method of forming a semiconductor structure comprising the steps of:
a) providing a semiconductor substrate;
b) providing a layer of SiGe over at least a region of the semiconductor substrate;
c) providing a mesa over a portion of the SiGe layer;
d) depositing a polycrystalline silicon layer over the mesa and over lower adjacent regions of the SiGe layer;
e) exposing an upper surface of the mesa by removing the polycrystalline silicon layer over the mesa; and,
f) removing the mesa to expose a region of SiGe below.

Claim 9 (withdrawn) A method as defined in claim 8, wherein the mesa is removed by an etching process.

Claim 10 (currently amended) A semiconductor device comprising:

a silicon substrate forming one of a collector and an emitter, the substrate being of a first conductivity type;
a layer of SiGe of a second conductivity type covering at least a portion of the silicon substrate;
a first layer of silicon of the second conductivity type at least substantially supported by and covering a substantial portion of the SiGe layer;
a first layer of polysilicon of the second conductivity type at least substantially supported by and covering a substantial portion of the first layer of silicon with the exception of a window region, the first layer of silicon entirely exposed within the window region and having its surface unaffected by a process of etching within the window region, the first layer of silicon forming a base terminal of the transistor; and,
a second layer of polysilicon of the first conductivity type insulated from the first layer of polysilicon and contacting the entirely exposed and unetched first layer of silicon within the window region, said second layer of polysilicon forming the other of the collector and the emitter terminals of the transistor.

Claim 11 (previously presented) A semiconductor device as defined in claim 10 wherein the silicon substrate comprises n-type material and forms the collector.

Claim 12 (previously presented) A semiconductor device as defined in claim 11 wherein the layer of SiGe comprises p-type material, and wherein the second layer of polysilicon comprises n-type material and forms the emitter.

Claim 13 (currently amended) A semiconductor device comprising:
a silicon layer of a first conductivity type;
a layer of SiGe of a second conductivity type covering at least a region of the silicon layer; and,
a first layer of silicon of the second conductivity type at least substantially supported by and covering a substantial portion of the silicon and SiGe layer;

a first layer of polysilicon of the second conductivity type at least substantially supported by and covering a substantial portion of the first layer of silicon with the exception of a small window region, within which the first layer of silicon is entirely exposed; and,
a second layer of polysilicon of the first conductivity type covering the small window region and entirely contacting the first layer of silicon within this small window region, where the first layer of silicon within the small window region has a surface unaffected by a process of etching.

Claim 14 (original) A semiconductor device as defined in claim 13, wherein the silicon layer serves as a substrate and is substantially thicker than the layer of SiGe.

Claim 15 (original) A semiconductor device as defined in claim 13 wherein the SiGe layer has a substantially uniform thickness.

Claim 16 (previously presented) A semiconductor device as defined in claim 13 wherein the thickness of the SiGe layer covered by the first layer of silicon is of a substantially same thickness and impurity concentration as the remaining portion of the layer of SiGe covering at least a region of the silicon layer.

Claim 17 (withdrawn) A method of applying a semiconductor seed layer to a mixed topology substrate having regions of exposed semiconductor material and regions of exposed dielectric material, comprising the steps of:
disposing the substrate in a growth chamber and nucleating the seed layer by exposing the semiconductor material and dielectric material to an atmosphere of gases, the gases being presented at a predetermined flow rate, temperature and pressure, wherein the temperature is less than 600 °C, the pressure is less than 10^{-2} mbar, and the flow rate is less than 5 sccm.

Claim 18 (withdrawn) A method as defined in claim 17 further comprising the step of cleaning surfaces of the substrate for removal of contamination and debris.

Claim 19 (withdrawn) A method as defined in claim 17 wherein at least one of the gases is hydrogen and has a flow rate of less than 500 sccm and wherein another of the gases is silane and has a reduced flow rate of less than 20 sccm and wherein said gases are injected into the deposition chamber to initiate the nucleation of silicon and produce the seed layer on all exposed surfaces.

Claim 20 (withdrawn) A method as defined in claim 17, wherein the seed layer is deposited to have a thickness of between 2 to 20nm.

Claim 21 (withdrawn) A method as defined in claim 17 wherein the seed layer is doped with impurities.

Claim 22 (previously presented) A semiconductor device according to claim 10, comprising an insulating material disposed between the two layers of polysilicon.

Claim 23 (previously presented) A semiconductor device according to claim 22, wherein the disposed insulating material is formed by reacting the first layer of polysilicon with a substance to form an insulating cover thereon.

Claim 24 (previously presented) A semiconductor device according to claim 22, wherein the disposed insulating material is formed by depositing an insulating material thereon.

Claim 25 (previously presented) A semiconductor device as defined in claim 10, wherein the first layer of silicon and the SiGe layer have a substantially uniform thickness.

Claim 26 (previously presented) A semiconductor device as defined in claim 10, wherein the thickness of the SiGe layer covered by the second layer of polysilicon is of a substantially a same thickness and impurity concentration as the remaining portion of the layer of SiGe covering at least a region of the silicon layer.

Claim 27 (previously presented) A semiconductor device according to claim 13, comprising an insulating material disposed between the two layers of polysilicon

Claim 28 (previously presented) A semiconductor device according to claim 27, wherein the disposed insulating material is formed by reacting the first layer of polysilicon with a substance to form an insulating film thereon.

Claim 29 (previously presented) A semiconductor device according to claim 27, wherein the disposed insulating material is formed by depositing an insulating material thereon.

Claim 30 (currently amended) A semiconductor device comprising:
a silicon substrate forming one of a collector and an emitter, the substrate being of a first conductivity type;
a layer of SiGe of a second conductivity type covering at least a portion of the silicon substrate;
a first layer of silicon of the second conductivity type at least substantially supported by and covering a substantial portion of the SiGe layer;
a first layer of polysilicon of the second conductivity type at least substantially supported by and covering a substantial portion of the first layer of silicon with the exception of a window region, the first layer of silicon entirely exposed within the window region and having its surface unaffected by a process of etching within the window region, the first layer of silicon forming a base terminal of the transistor; and,
a second layer of polysilicon of the first conductivity type insulated from the first layer of polysilicon and contacting the unetched first layer of silicon within the window region in its entirety, said second layer of polysilicon forming the other of the collector and the emitter terminals of the transistor, wherein the first silicon ~~layer~~ layer has a uniform thickness profile in a direction transverse the layers within the semiconductor substrate within predetermined limits within a region of the semiconductor substrate including at

least a transistor, the uniform thickness profile for providing substantially reproducible results for the thickness of the first silicon ~~layer~~ layer.

Claim 31 (previously presented) A semiconductor device as defined in claim 30, wherein the uniform thickness profile provides substantially reproducible electrical characteristics of the first silicon layer and the SiGe layer.

Claim 32 (previously presented) A semiconductor device as defined in claim 31, wherein the uniform thickness profile of the SiGe layer is other than a uniformly thick layer.